Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (original) A process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate which comprises:

a) forming a test pattern in selected fields of a first layer on a semiconductor substrate;

b) forming a layer of photoresist over said first layer;

c) forming latent images in portions of said photoresist layer lying in said selected fields overlying said test pattern of said first layer; and

d) measuring the alignment of said test pattern in said selected fields of said first layer with said overlying latent images in said photoresist layer using scatterometry.

2. (previously amended) The process of claim 1 wherein said step of forming a test pattern in said selected fields of said first layer comprises forming a test pattern of lines.

3. (previously amended) The process of claim 2 wherein said step of forming a test pattern of lines in said selected fields of said first layer comprises a test pattern of parallel spaced apart lines.

4. (previously amended) The process of claim 2 wherein said step of forming said test pattern of lines formed in said selected fields of said first layer comprises forming a test pattern of parallel spaced apart metal lines.

5. (previously amended) The process of claim 3 wherein said step of forming latent images in said portions of said photo resist layer lying in said selected fields overlying said test pattern of lines comprises forming a pattern of parallel spaced apart lines.

6. (previously amended) The process of claim 5 wherein said step of forming said latent images of parallel spaced apart lines, in said portions of said photoresist layer lying in said selected fields overlying said test pattern of parallel spaced apart lines in said selected fields of said first layer, further comprises forming said latent images of said parallel spaced apart lines generally parallel to said test pattern of parallel spaced apart lines formed in said selected fields of said upper layer, whereby said test pattern of parallel spaced apart lines formed in said selected fields of said under layer and said latent images of parallel spaced apart lines formed in said portions of said photoresist layer lying in said selected fields form a diffraction grating, the accuracy of which is measured by said scatterometry to determine the alignment of said layers of lines.

7. (previously amended) The process of claim 6 wherein said step of forming said latent images of parallel spaced apart lines further comprises interspacing said latent images of parallel spaced apart lines between said test pattern of parallel spaced apart lines formed in said selected fields of said first layer.

8. (original) A process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate which comprises:

a) forming a test pattern of parallel spaced apart lines in selected fields of a first layer on a semiconductor substrate;

b) forming a layer of photoresist over said first layer;

c) forming latent images of parallel spaced apart lines in portions of said photo resistlayer lying in said selected fields overlying said test pattern of parallel lines of said first layer, said parallel lines of said test pattern of said first layer generally parallel with said parallel lines of latent images in said photoresist layer; and

d) measuring the alignment of said parallel lines of said test pattern in said selected fields of said first layer with said overlying latent images of parallel lines in said photoresist layer using scatterometry.

9. (previously amended) The process of claim 8 wherein said step of forming a test pattern of parallel spaced apart lines in said selected fields of said first layer comprises forming a test pattern of parallel spaced apart metal lines.

10. (previously amended) The process of claim 8 wherein said step of forming said latent images of parallel spaced apart lines in said photoresist layer and said test pattern of parallel spaced apart lines in said first layer comprises forming said latent images and said test pattern [are formed] generally parallel to one another to form a diffraction grating, the accuracy of which is measured by said scatterometry to determine the alignment of said layers of lines.

11. (original) The process of claim 10 wherein said latent images of parallel spaced apart lines are interspaced between said test pattern of parallel spaced apart lines formed in said first layer.

12. (original) The process of claim 8 wherein said step of forming latent images of parallel spaced apart lines in said photoresist layer further comprises directing a first source of radiation onto said photoresist layer through a reticle patterned to provide a radiation image of said parallel spaced apart lines on said photoresist layer.

13. (original) The process of claim 12 wherein said step of measuring the alignment of said parallel lines of said test pattern in said selected fields of said first layer with said overlying latent images of parallel lines in said photoresist layer using scatterometry further comprises directing a second source of radiation toward said latent images of lines in said photo resist layer and toward said test pattern of parallel spaced apart lines in said first layer.

14. (original) The process of claim 12 wherein said first source of radiation used to form said latent images in aid photoresist layer comprises ultraviolet light.

15. (previously amended) The process of claim 13 wherein said second source of radiation used in said scatterometry to determine said alignment comprises visible light.

16. (previously amended) The process of claim 13 wherein said second source of radiation used in said scatterometry to determine said alignment comprises a radiation source selected from the group consisting of an electron beam, an ion beam, and a laser beam.

17. (Previously cancelled).

18. (original) A process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate which comprises:

a) forming a test pattern of parallel spaced apart metal lines in selected fields of a first layer on a semiconductor substrate;

b) forming a layer of photoresist over said first layer;

c) forming latent images of parallel spaced apart lines in portions of said photoresist layer lying in said selected fields overlying said test pattern of parallel lines of said first layer, said parallel lines of said test pattern of said first layer generally parallel with said parallel lines of latent images in said photoresist layer;

d) measuring the alignment of said parallel lines of said test pattern in said selected fields of said first layer with said overlying latent images of parallel lines in said photoresist layer using scatterometry; and

e) forming a further layer of integrated circuit structure over said first layer on said integrated circuit structure in fields not used for said alignment.

19. (Previously cancelled).

20. (previously presented) A process for measuring alignment of latent images in selected fields of a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in said selected fields on an upper layer on the substrate underlying said photoresist layer which comprises:

a) forming a test pattern in said selected fields of said upper layer on said semiconductor substrate;

b) forming a layer of photoresist over said upper layer;

c) forming latent images in portions of said photoresist layer lying in said selected fields of said photoresist layer overlying said test patterns in said selected fields of said upper layer; and

d) measuring the alignment of said test patterns in said selected fields of said upper layer with said overlying latent images in said selected fields in said photoresist layer using scatterometry;

whereby alignment of said test pattern in said selected fields in said upper layer on said semiconductor substrate with said latent images in said selected fields of said photoresist layer permits the remaining fields in said semiconductor substrate to be conventionally processed to form semiconductor structures.

21. (previously presented) The process of claim 20 wherein said step of forming a test pattern in said selected fields of said upper layer on said semiconductor substrate further comprises forming a test pattern of parallel spaced apart metal lines in said selected fields of said upper layer on said semiconductor substrate; and said step of forming latent images in portions of said photoresist layer lying in said selected fields of said photo resist layer overlying said test patterns in said selected fields of said upper layer further comprises forming latent images in said photoresist layer comprising a test pattern of parallel spaced apart metal lines.